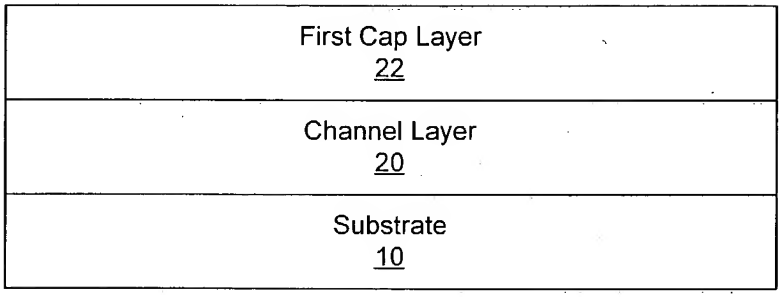

Figure 1A

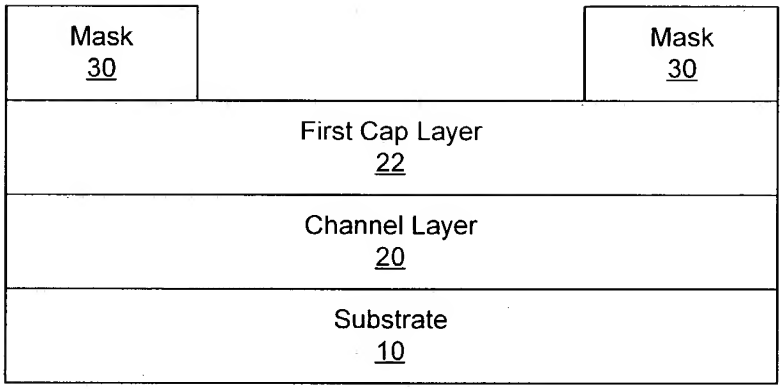

Figure 1B

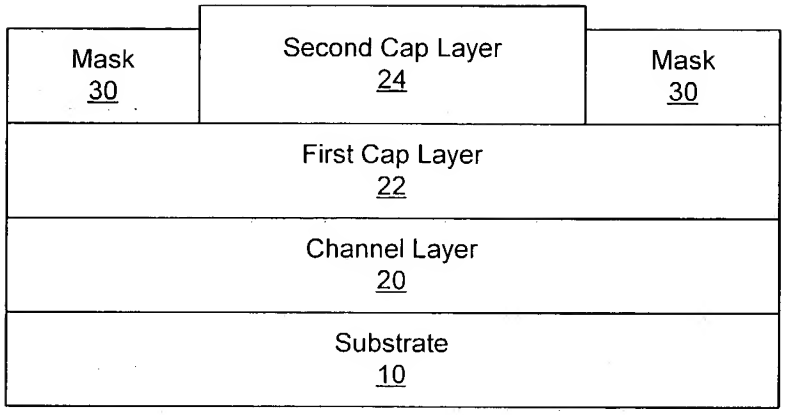

Figure 1C

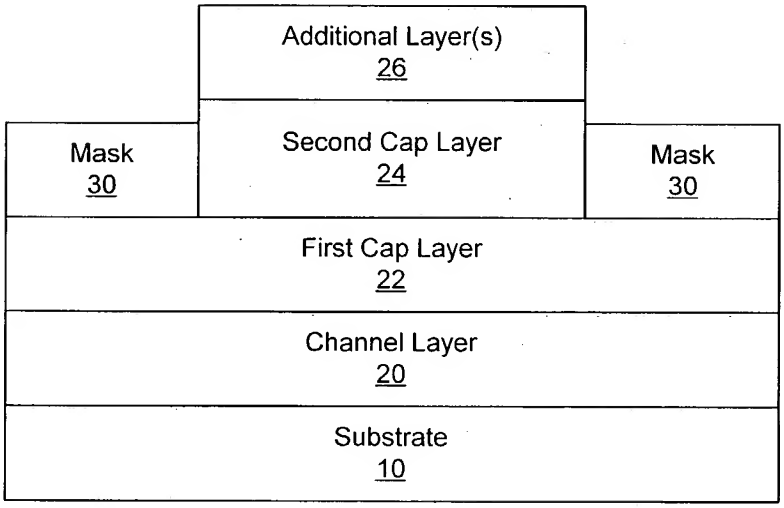

Figure 1D

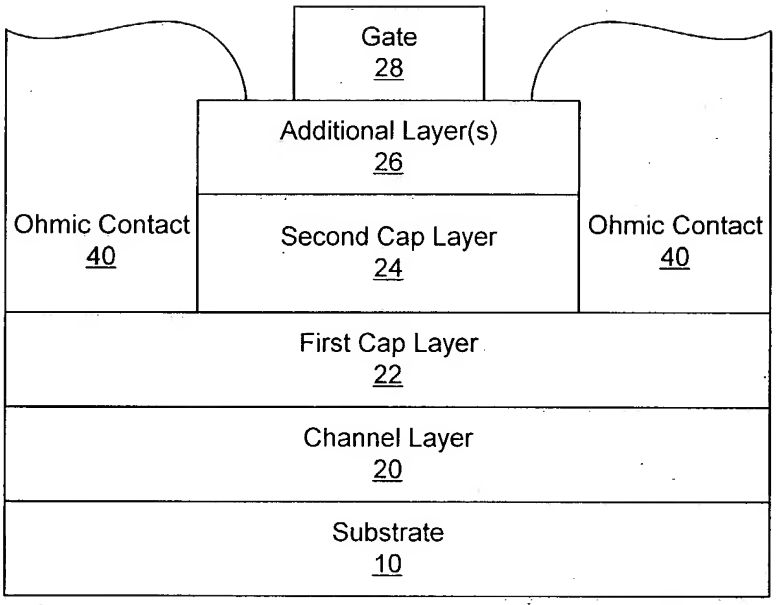
Gate
28
Additional Layer(s)
26
Ohmic Contact
40
Second Cap Layer
24
Ohmic Contact
40
First Cap Layer
22
Channel Layer
20
Substrate
10

Figure 1E

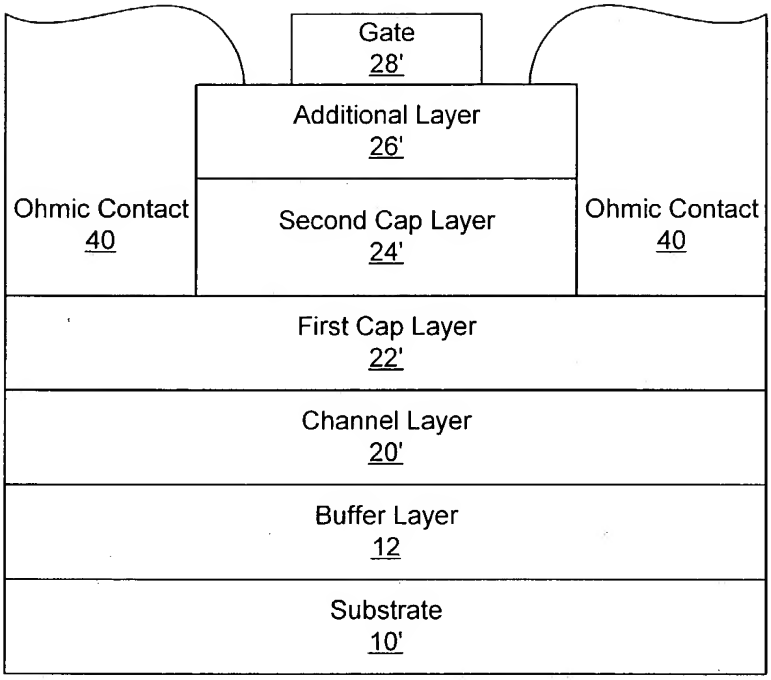
Gate
28'
Additional Layer
26'
Ohmic Contact
40
Second Cap Layer
24'
Ohmic Contact
40
First Cap Layer
22'
Channel Layer
20'
Buffer Layer
12
Substrate
10'

Figure 2

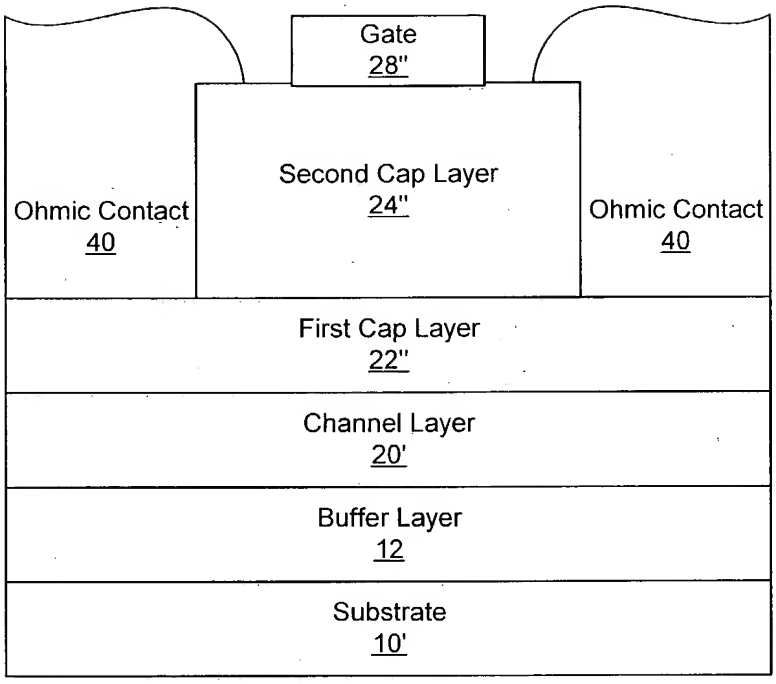
Gate
28''
Second Cap Layer
24''
Ohmic Contact
40
Ohmic Contact
40
First Cap Layer
22''
Channel Layer
20'
Buffer Layer
12
Substrate
10'

Figure 3

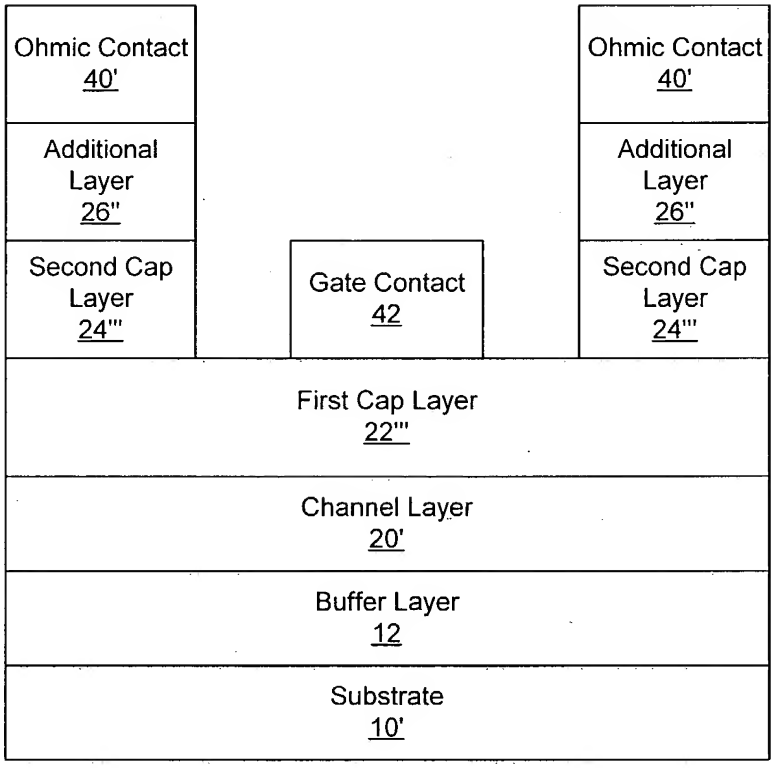
Ohmic Contact
40'
Ohmic Contact
40'
Additional
Layer
26"
Additional
Layer
26"
Second Cap
Layer
24'''
Gate Contact
42
Second Cap
Layer
24'''
First Cap Layer
22'''
Channel Layer
20'
Buffer Layer
12
Substrate
10'

Figure 4

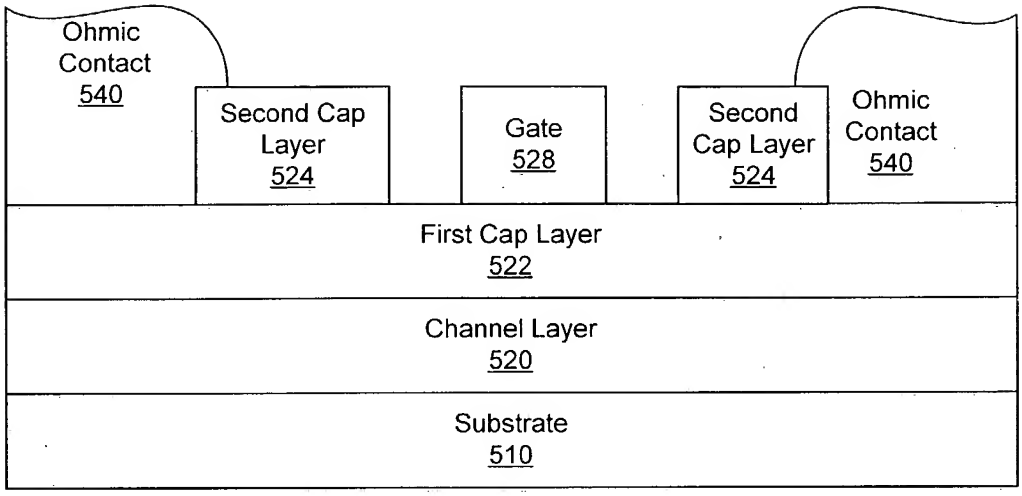
Ohmic
Contact
540
Second Cap
Layer
524
Gate
528
Second
Cap Layer
524
Ohmic
Contact
540
First Cap Layer
522
Channel Layer
520
Substrate
510

Figure 5

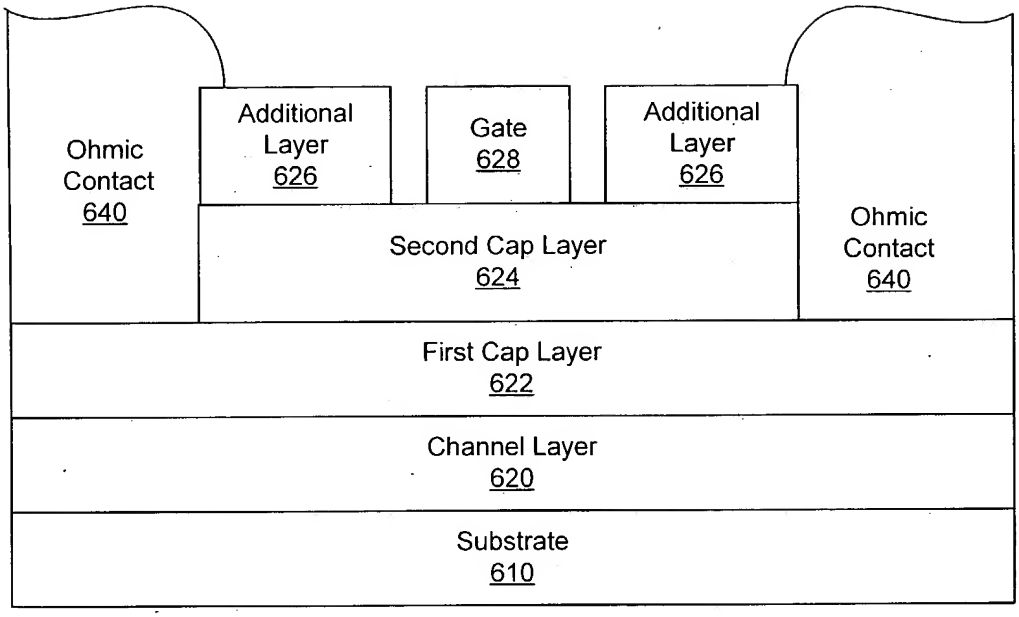
Ohmic Contact 640
Additional Layer 626
Gate 628
Additional Layer 626
Second Cap Layer 624
Ohmic Contact 640
First Cap Layer 622
Channel Layer 620
Substrate 610

Figure 6